THE UNIVERSITY OF WAIKATO
Department of Computer Science

COMP311 — Advanced Computer Architecture 2008
Assignment 3 - VHDL PC

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Due:	6 Oct 2008
Worth:	5%

For this assignment you are going to design and simulate a program counter (PC) as found in a simple CPU. You are to model your design in VHDL and simulate it using Riviera.

A top-level block diagram for the PC is shown in Figure 1. The *increment* input causes one to be added to the PC value. When the *load* input is asserted the value of the PC is loaded from the *in* lines. When the *output enable* asserted the current value of the PC is placed on the *out* lines. At other times, the *out* lines should be high impedance.

You should use a hierarchical approach to your design. Do not use VHDLs add functionality to do the addition, instead include logic to perform the addition. You do not need to model propagation delays.

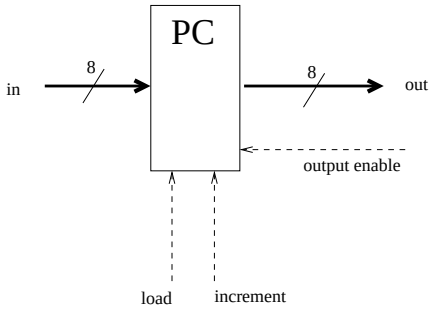

Figure 1: Top-Level Block Diagram for the Program Counter

Submit your assignment on moodle. You should hand in the following:

1. A block diagram showing the internal structure of your PC
2. Your VHDL files including your test bench
3. Details on how to compile and run simulations of your PC. You should also describe any assumptions that you made in your interpretation of the specification.