COMP311-07B MID-SEMESTER TEST

DEPARTMENT:	Computer Science
PAPER TITLE:	Computer Systems Architecture
TIME ALLOWED:	90 minutes
TOTAL MARKS:	90 marks
NUMBER OF QUESTIONS IN PAPER:	Eleven
NUMBER OF QUESTIONS TO BE ANSWERED:	Eleven
VALUE OF EACH QUESTION:	The value of each question is noted.
GENERAL INSTRUCTIONS:	Answer ALL ELEVEN questions.
SPECIAL INSTRUCTIONS:	If possible, write your answers in the spaces provided. Additional paper is available, should you require it.
CALCULATORS PERMITTED:	Yes

The University of Waikato
Te Whare Wānanga o Waikato

NAME OF STUDENT:

1. Two MIPS design principles are 'simplicity favours regularity' and 'good design demands good compromises'. Provide an example of each using the MIPS architecture.

[6 marks]

2. A simple ALU unit for a MIPS CPU can be built using a ripple adder. Draw a 4-bit ripple adder that supports subtraction, the set-if-less-than instruction, overflow detection, and a test for equality. Note: your answer does not have to show the internals of each 1-bit adder; it should, however, show how signals are forwarded as well as control lines.

[12 marks]

3. Multiplication can be accomplished using a combination of shifting and addition.

   (a) Multiply 0101 by 1011 showing all intermediate steps, in binary.

   [2 marks]

   (b) Draw a multiplier unit that is capable of completing this multiplication. Your unit will comprise of an 8-bit product register, an 8-bit ALU, an 8-bit multiplicand register, a 4-bit multiplier register, and a control test.

   [4 marks]

4. Using the following components, draw a single-cycle datapath capable of executing R-type instructions, as well as lw and sw. Note: your datapath does not need to show the fetch or decode logic, nor does it have to show a control unit.

[14 marks]
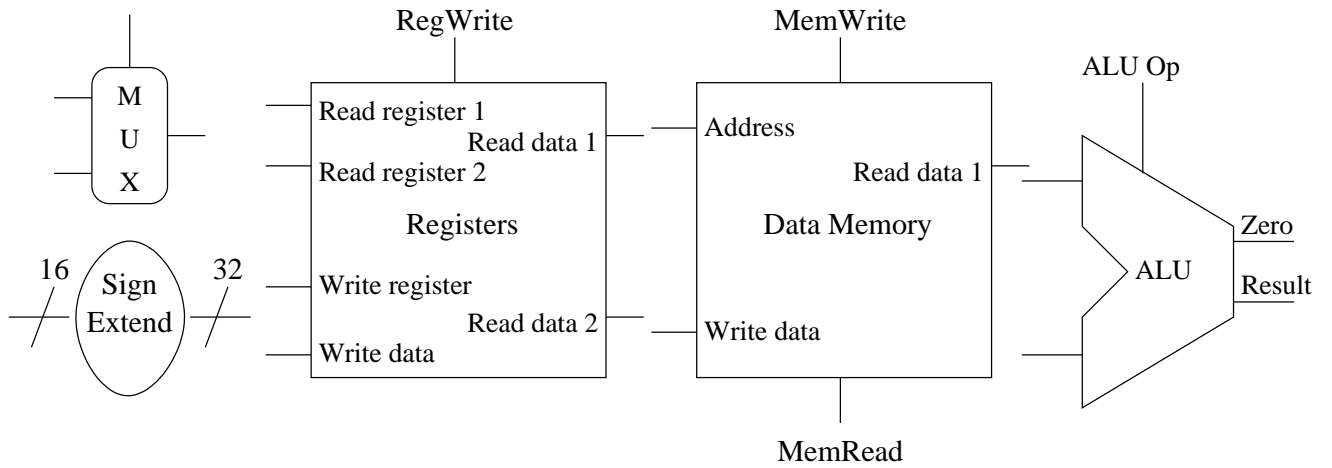
5. To reduce the delay of the branch instruction, some architectures move the equality test from the execute stage to the decode stage.

   (a) outline a faster, more efficient test for equality that does not use subtraction. provide examples to show how it works.

   [6 marks]

   (b) draw a diagram that illustrates how the equality test is logically connected to other components in the decode stage of the MIPS 5-stage pipelined datapath.

   [2 marks]

6. What dependencies exist in the following 5 MIPS instructions? Which dependencies are hazards, assuming a 5-stage IF/ID/EX/MEM/WB pipeline?

```
add $3, $1, $2
lw  $4, 0($3)
sub $5, $4, $3
or  $6, $3, $1
sw  $5, 0($3)
```

[8 marks]

7. The IEEE 754 floating point standard specifies that a C float consists of a sign bit, 8 bits of exponent with a bias of 127, and 23 bits of significand.

   (a) What is the purpose of an exponent bias? That is, why not just use two's complement to represent the exponent?

   [2 marks]

   (b) Show the result, in floating point binary, of adding the following two floating point numbers.

```
00111111111100000000000000000000
01000000001000000000000000000000
```

   [10 marks]

8. Three techniques to improving processor performance are super-pipelining, super-scalar, and dynamic pipelining. Using examples, describe each of these techniques.

[6 marks]

9. Some CPU architectures, such as the Alpha, include conditional move instructions. For example, cmoveq $4, $5, $6 will store the value held in register $5 in register $6 if register $4 is equal to zero.

   (a) what is the equivalent MIPS instruction sequence? Hint: your answer should show three instructions.

[4 marks]

   (b) what are the two main advantages of a conditional move instruction?

[4 marks]

10. Some CPU architectures, such as the SPARC, provide a register window. What is a register window? How is one used?

[4 marks]

11. Some CPU architectures require memory accesses to be aligned.

   (a) If an architecture has a word size of 32 bits, outline a logic test to see if a particular value is word-aligned.

   [2 marks]

   (b) What is the range of branch distances on this machine, assuming a 16-bit immediate value?

   [4 marks]