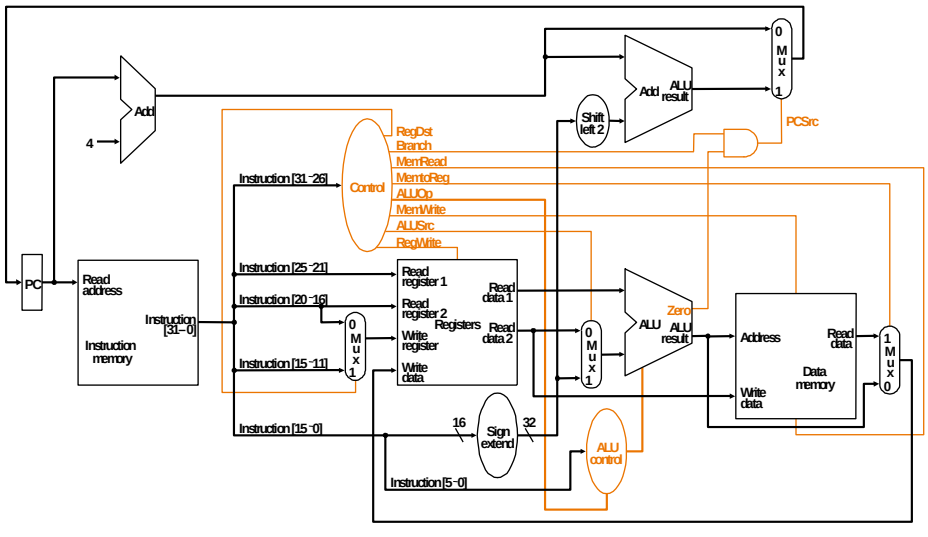
Datapath Design II

Datapath with Control Unit



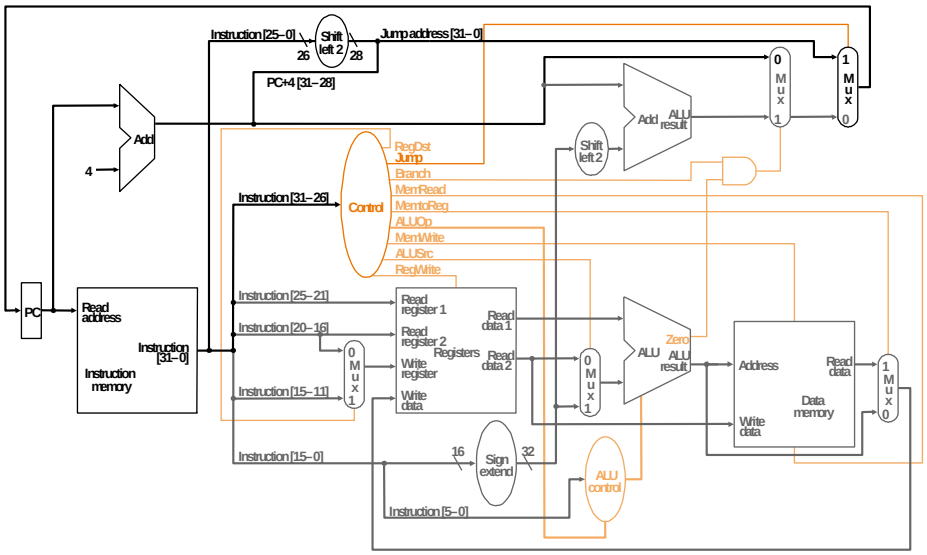
Operation of Datapath

Instruct	Reg Dst	ALU Src	Mem toReg	Reg Write	Mem Read	Mem Write	Branch	ALU Op1	ALU Op0
R-Type									
lw									
sw									
beq									

Example

- What is necessary to extend the Datapath to allow the Jump Instruction to be executed?

Jump Instruction



What not use a Single Cycle Implementation?

- Every clock cycle is of equal length
  - CPI = 1
  - Clock cycle time determined by longest path (almost certainly load instruction in our datapath)

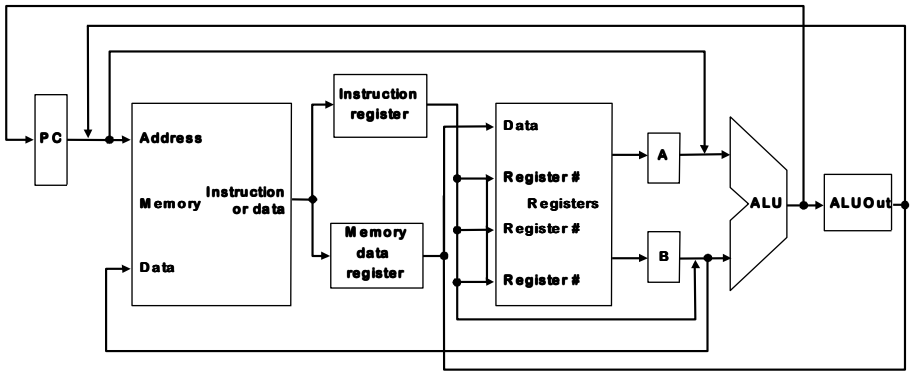
Example

- Which of the following implementations would be faster and by how much
  - Implementation which uses a fixed length clock cycle
  - Implementation where clock cycle length determined by instruction
- Assume:
  - Memory units have 2ns delay
  - ALU and adders have 2ns delay
  - Register file has 1ns delay
  - All other units have 0 delay
- Assume following instruction mix:
  - 24% loads
  - 12% stores
  - 44% R-Type
  - 18% branches
  - 2% Jumps

MultiCycle Implementation

- Instruction execution can be broken into the following steps
  - Instruction Fetch
  - Instruction Decode
  - Operand Fetch
  - Execute
  - Store Results
- Also allows sharing of components
  - single memory for data and instructions
  - Single ALU
- Extra registers required to store results between stages

High Level Datapath



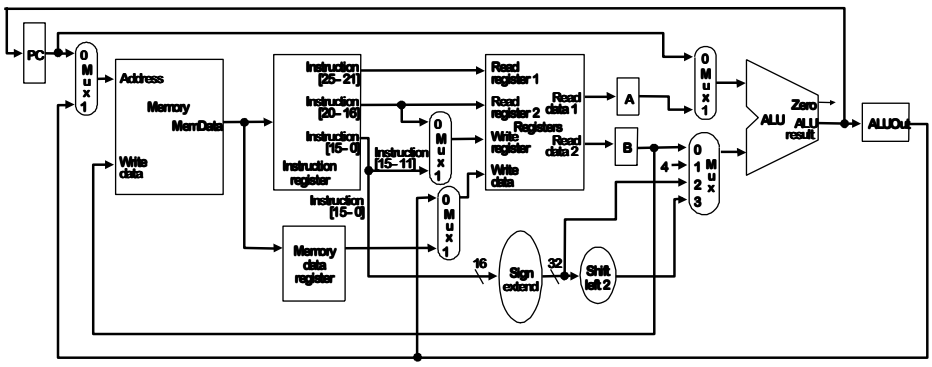
Additional Registers

- Determined by:
  - What combination units can fit in a clock cycle
  - What data is required in later clock cycles
- Assume at most one of the following can be accommodated by a single clock cycle:
  - A memory access
  - A register file access (two reads or one write)
  - An ALU operation
- Require the following additional registers
  - IR
  - MDR
  - A and B registers
  - ALUout register
- All new regs except IR only have to hold values from one clock cycle to next so do not require write control signal

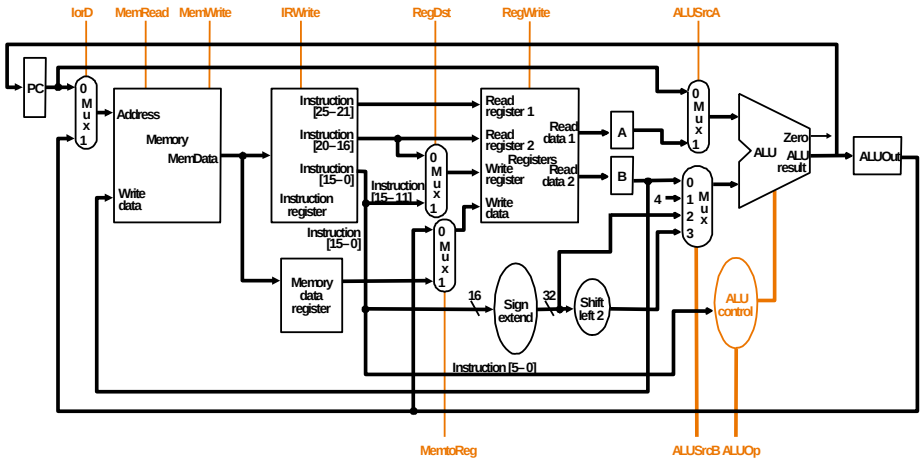
Combining ALUs

- Merging all ALUs and adders into a single datapath requires two main changes:
  - An additional multiplexer on the A input to the ALU, selects:
    - PC
    - A register
  - Extend multiplexer on second input
    - The constant 4 for incrementing PC
    - The sign extended and shifted 16-bit offset field used in branch address computation

Datapath



Datapath with Control Signals



Completed Datapath